Claims:

1. A method of interleaving a data stream comprising:

writing a sequence of groupings of bits from the data stream, the groupings having a predetermined size, from a data bus into a memory;

applying selected groupings read from the memory to a first multiplexer (MUX);

applying the groupings applied to the first MUX to a second MUX; and

applying at least one grouping to the second MUX between applying groupings from the first MUX to the second MUX.

2. The method of claim 1, wherein the memory comprises a first-in, first-out memory (FIFO).

3. The method of claim 1, wherein each of the groupings comprises a byte.

4. The method of claim 1, wherein said at least one grouping comprises bits representing a virtual local area network (VLAN) tag.

5. The method of claim 4, wherein said at least one grouping comprises bits originating from another data stream.

6. The method of claim 0-1, wherein writing a sequence of groupings of bits into a memory comprises receiving a consecutive sequence of groupings of bits and writing the consecutive sequence into the memory.

7. The method of claim 6, wherein receiving a consecutive sequence of groupings of bits and writing the consecutive sequence into the memory comprises receiving bursts of data signals and writing the received bursts of data signals to the memory.

8. The method of claim 6, wherein the bursts of data signals are provided via the data bus from at least one burst-mode memory.

9. The method of claim 8, wherein the at least one burst mode memory comprises at least one burst mode dynamic random access memory (DRAM).

10. The method of claim 1, wherein applying selected groupings read from the memory to a first MUX comprises selecting, from the stored groupings, groupings that represent signal information other than a virtual local area network (VLAN) tag.

11. The method of claim 1, wherein applying groupings read from memory to the first MUX occurs a grouping at a time.

12. An integrated circuit (IC) comprising:

a memory, a plurality of multiplexers (MUXes), and a state machine;

said memory, MUXes and state machine being coupled so that, responsive to applied control signals, selected groupings of bits from a received bit stream are capable of being extracted to produce another bit steam different from the received bit stream.

13. The IC of claim 12, wherein said state machine comprises a memory extraction state machine.

14. The IC of claim 12, wherein said memory comprises a first-in, first-out memory (FIFO).

15. The IC of claim 12, wherein said memory and MUXes are further coupled so that, responsive to additional applied control signals, at least one selected grouping from another data stream may be inserted to produce a bit stream different from the received bit stream.

16. The IC of claim 15, wherein said memory comprises a first-in, first-out memory (FIFO), and said state machine comprises a FIFO extraction state machine.

17. The IC of claim 15, wherein said memory is adapted to receive said received bit stream in bursts of data signals.

18. A system comprising: a computer adapted to be coupled to an ethernet compliant network; said computer including an integrated circuit; the integrated circuit comprising a memory, a plurality of multiplexers (MUXes) and a state machine; said memory, MUXes, and state machine being coupled so that, responsive to applied control signals, selected groupings of bits from a received bit stream are capable of being extracted to produce another bit stream different from the received bit stream.

19. The system of claim 18, wherein said memory and MUXes are further coupled, so that, responsive to additional control signals, at least one selected grouping from another data stream may be inserted to produce yet another bit stream different from the received bit stream.